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PTO/SB/21 (04-04)
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/024,936
Filing Date	18 December 2001
First Named Inventor	Joel Wayne Davenport
Art Unit	2827
Examiner Name	L. Cruz
Total Number of Pages in This Submission: 35	Attorney Docket Number: US 018102

ENCLOSURES *(Check all that apply)*

- [X] Fee Transmittal Form
- [X] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)** (in triplicate)
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Other Enclosure(s) (please Identify below): 2 return post cards

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Raymond J. Werner
Signature	Raymond J. Werner Reg. No. 34,752
Date	22 July 2004

CERTIFICATE OF TRANSMISSION/MAILING

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Signature	Kathryn G Nelson	Date	22 July 2004

PTO/SB/17 (10-03)
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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330 —

Complete if Known	
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METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

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☐ Charge fee(s) indicated below ☐ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) Ø

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X	=
Independent Claims		- 3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) Ø

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	47	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330 —
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1, 30	2453	66	Petition to revive - unintentional	
1501	1, 30	2501	66	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	38	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	38	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	38	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330 —

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Raymond J. Werner	*Registration No. (Attorney/Agent)*	34,752	*Telephone*	503-466-2994
Signature	Raymond J Werner			*Date*	22 July 2004

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant	:	Joel Wayne Davenport, et al.	;	
Appl. No.	:	10/024,936	;	Grp./Art Unit : 2827
Filed	:	18 December 2001	;	Examiner: L. Cruz
			;	
Title	:	Single Package Containing Multiple Integrated Circuit Devices	;	
			;	
Docket No.	:	US018102	;	

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

This Appeal Brief is being filed in response to the Examiner's Final Rejection of Claims 1-7 and 13-17. A Notice of Appeal was filed on 22 May 2004.

Real Party In Interest

The real party in interest in this application is Koninklijke Philips Electronics N.V., which is the assignee of this application, and which is also the parent company of Philips Electronics North America Corporation.

Related Appeals or Interferences

Applicant is not aware of any related appeals or interferences.

Status of Claims

Claims 1-7 and 13-17 are pending in the application, Claims 8-12 were previously cancelled, and all the pending Claims 1-7 and 13-17 have been finally rejected.

Status of Amendments

All amendments are believed to have been entered. Responsive to Applicants' After Final Response and Amendment of 14 April 2004, an Advisory Action dated 03 May 2004 indicates that, for purposes of Appeal, the amendment submitted on 14 April 2004 will been entered.

Summary of the Invention

The present invention relates generally to apparatus for packaging multiple integrated circuits that operate at different voltages in a single package. More particularly, a ball-grid array (BGA) package, which includes multiple layers of conductors separated by dielectric layers, is arranged such that the power planes, ground planes, and connection balls associated with each of at least two integrated circuits are separated from each other by at least a distance that is based upon the difference in operating voltages between the integrated circuits.

Issues

The first issue presented on appeal is whether Claims 1-7 have been properly rejected under 35 USC §103(a) over Koepf (US Patent 5,138,436) in view of Cadence (Allegro Designer/Allegro Expert).

The second issue presented on appeal is whether Claims 13-17 have been properly rejected under 35 USC §103(a) over Koepf (US Patent 5,138,436) in view of Cadence (Allegro Designer/Allegro Expert).

Grouping of Claims

Claims 1-7 may be grouped together.

Claims 13-17 may be grouped together.

Arguments

Claims 1-7 and 13-17 have been rejected under 35 USC §103(a) as being unpatentable over KOEPF (US Patent 5,138,436) in view of CADENCE (Allegro Designer/Allegro Expert, Power Solutions for Today's PCB Challenges). The Examiner applies the same arguments to Claims 1-7 and 13-17.

The disclosure of KOEPF relates generally to a package assembly for electronic circuits, and more particularly relates to replacing wire bonds with an interconnect member that overlays an integrated circuit and electrically connects a plurality of contact pads on the integrated circuit to a corresponding plurality of electrically conductive paths on the interconnect member. The electrically conductive paths of the interconnect member are further connected to contact pads disposed on an I/O substrate. KOEPF discloses that connections between the interconnect member and the integrated circuit may be made through the use of solder bumps. The I/O substrate is disposed on a chip carrier, and has openings, or recesses, therein. The integrated circuit is also disposed on the chip carrier, and more particularly is disposed in an opening, or recess, of the I/O substrate. In the package assembly of KOEPF, the top surfaces of the I/O

substrate and the integrated circuit are substantially coplanar, and the interconnect member serves as a bridge to provide electrically conductive paths between the I/O substrate and the integrated circuit. KOEPF further discloses that a sealing lid is disposed over the integrated circuit and I/O substrate. In such a configuration the I/O substrate is disposed intermediate the chip carrier and the sealing lid. External connections to the package assembly of KOEPF are made by way of contacting conductive leads on the I/O substrate that extend out beyond the sealing lid.

The Examiner cites KOEPF for a disclosure of a BGA package. Applicants respectfully submit that there is no teaching in KOEPF of a ball grid array (BGA) package as is claimed in independent Claims 1 or 13. A BGA package in accordance with the claimed invention is illustrated in Figs. 2A and 2B of the present application, and has a major surface, typically thought of as the "bottom" of the BGA package, on which a number of external electrical connection contacts are disposed. These external electrical connection contacts take the form of solder balls arranged in a grid-like array. However, as described in the preceding paragraph, the package assembly of KOEPF does not have such external electrical connection contacts. Although KOEPF does disclose the use, internal to a package, of solder bumps, between an interconnect member and an integrated circuit, this is clearly different than a BGA package in which solder balls (in contradistinction to solder bumps which are recognized as being smaller than solder balls) are disposed in a grid-like array on an external surface of a package so as to form external connection contacts. KOEPF does not disclose, suggest, or provide motivation for a BGA package as claimed.

The Examiner cites KOEPF for a disclosure of a BGA package having a plurality of external connection contacts on **28** and on **15**. Applicants respectfully submit the elements **28** and **15** referred to by the Examiner have been mischaracterized as disclosing the external connection contacts of a BGA package, and that KOEPF does not provide any teaching of a BGA package having a plurality of external connection contacts. Firstly, element **28** of KOEPF is the interconnect substrate, which is a component that is internal to the KOEPF

package. As an internal element it is not possible for element **28** to disclose external connection contacts of a BGA package. Secondly, element **15** is the I/O substrate of the KOEPF package, which does have leads disposed thereon which lie outside the seal ring and sealing lid of the KOEPF package. However, this can not be used as a disclosure of the external connection contacts of a BGA package, since (a) no solder balls are shown on these leads; (b) these leads are disposed only at peripheral locations of the KOEPF package, which is unlike the "array" of a ball grid array package (see Applicants' Figs. 2A and 2B); and (c) these leads are disposed on an intermediate layer of the KOEPF package, as opposed to an outer major surface as illustrated in Applicants' Figs. 2A and 2B.

The Examiner cites KOEPF for a disclosure, as set forth in Claim 1, of a first device, having a plurality of electrical connections connected to a first set of the external electrical connection contacts; and a second device having a plurality of electrical connections connected to a second set of the external electrical connection contacts; wherein the first and second sets of the external electrical connections are segregated in two sections which are electrically isolated from each other. Applicants respectfully submit that there is no such teaching in KOEPF. What KOEPF actually discloses is that RF lines and DC lines may be segregated from each other. However, KOEPF does not disclose that: (a) the electrical connections of a first device are connected to a first group of external connection contacts, (b) the electrical connections of a second device are connected to a second group of external connection contacts; and (c) the first and second groups (associated respectively with the first and second devices) are segregated from each other. KOEPF discloses segregation based on signal type, not the segregation recited in Claim 1 wherein each of the segregated groups of external connections is associated with a particular device.

Additionally, with respect to independent Claim 13, KOEPF does not disclose a BGA package having a plurality of layers of conductors, wherein each of the plurality of layers are segregated into sets of conductors with the sets on each layer are spaced apart from each other, and the sets are adapted for connection to different integrated circuits. In fact, KOEPF teaches away from this

aspect of Applicants' Claim 13. More particularly, KOEPF discloses a ground plane that is common to all of the integrated circuits disposed on the chip carrier (see the package ground plane **14**). Additionally, the Examiner has mischaracterized element **24** of KOEPF as a power layer, when it is actually an I/O interconnect.

The Examiner states that KOEPF is silent about separating electrically isolated sections by a first distance based upon an expected Voltage difference, and cites CADENCE for a teaching of voltage dependent spacing for BGA package construction. Applicants respectfully submit that there is no teaching of voltage dependent spacing for BGA package construction as set forth by Applicants' Claims in CADENCE.

There is a mention of a BGA package in CADENCE in connection with a graphical wizard facility in the Cadence software, wherein the graphical wizard is intended to provide greater ease-of-use for designers. The actual sentence is:

> "Allegro's IntelliUSE employs an innovative graphical wizard to help streamline and simplify many complex procedures, such as multilayer padstack design, BGA package construction, user environment variable settings and design rule error location and debug."

Applicants respectfully submit that this aspect of CADENCE, does not disclose, suggest, or provide motivation for BGA package assembly as defined by independent Claims 1 or 13.

Furthermore, the only mention of voltage dependent spacings in the CADENCE is in connection with that portion of the Cadence software tool suite that routes signal lines, i.e., interconnect paths. More particularly, CADENCE, in connection with a push/shove router, discloses only that a path can be routed such that obstacles are pushed aside from the interconnect path, or that the interconnect path is made to contour-follow other interconnect as a priority, and only pushes aside or jumps obstacles when it has no other choice. The actual sentence is:

> "The shape-based, push-and-shove capability follows all complex rules regarding line widths and voltage-dependent spacings."

Applicants respectfully submit that this aspect of CADENCE, does not disclose, suggest, or provide motivation for BGA package assembly as defined by independent Claims 1 or 13.

Applicants do not simply claim two conductors in a BGA package that are spaced apart from each other. Applicants' independent Claim 1 is clearly directed to packages in which a first and a second set of external electrical connection contacts are segregated into respective first and second sections, and those sections, containing the external electrical connection contacts, are separated from each other by at least a distance that is based on the difference in operating voltage of the electrical devices connected, respectively, to those sets of external electrical contacts. Similarly, Applicants' independent Claim 13 is directed to ball grid array packages in which each of a plurality of layers in the BGA package includes a plurality of sets of electrical conductors that are segregated into a corresponding plurality of electrically isolated sections, with the sections being separated by a minimum distance based on an expected voltage difference between the sets of electrical conductors.

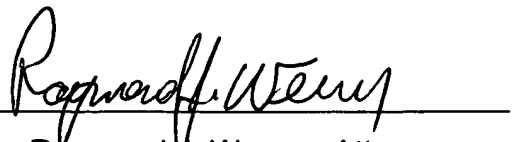
Additionally, with respect to CADENCE, Applicants note that the Examiner dates this reference as being from 1985 on the form PTO-892 provided with the Office Action of 24 February 2004. However, the copyright notice found in CADENCE actually identifies the material therein as being from the period 1985 through 2001. The Examiner has not established whether any of the allegedly relevant material actually predates Applicants' priority date of 09 July 2001.

Conclusion

The rejections of Claims 1-7 and 13-17 under 35 USC §103(a) as being unpatentable over KOEPF in view of CADENCE are thus believed to be improper

and should be REVERSED, which is respectfully urged.

Respectfully submitted,

By 

Dated: 22 July 2004
Hillsboro, Oregon

Raymond J. Werner, Attorney
Reg. No. 34,752

APPENDIX OF PENDING CLAIMS

1. A ball grid array (BGA) package assembly having a plurality of external connection contacts, comprising:

a first device, disposed on the BGA package, and having a plurality of electrical connections connected to a first set of the external electrical connection contacts; and

a second device, disposed on the BGA package, and having a plurality of electrical connections connected to a second set of the external electrical connection contacts;

wherein the first and second sets of the external electrical connections are segregated in two sections which are electrically isolated from each other, and the two sections are separated by at least a first distance wherein the first distance is based upon an expected difference in operating voltage between the first device and the second device.

2. The package of claim 1, wherein the first distance is in accordance with a predetermined standard.

3. The package of claim 2, wherein the standard specifies a physical separation distance between conductors based at least upon a voltage between the conductors.

4. The package of claim 1, further comprising:

a plurality of layers, including a signal layer, a power layer, a ground layer and a bottom layer;

wherein each of the layers includes two sets of electrical connections that are segregated in two sections which are electrically isolated from each other, and the two sets of electrical connections are respectively connected to the first and second devices.

5. The package of claim 4, wherein the standard specifies a physical separation distance between conductors based at least upon a voltage between the conductors.

6. The package of claim 1, wherein the first and second devices are semiconductor integrated circuit (IC) devices.

7. The package of claim 6, wherein the IC devices are communications devices.

13. A ball grid array package, comprising:

a plurality of layers, including a signal layer, a power layer, a ground layer and a bottom layer;

wherein each of the layers includes a plurality of sets of electrical conductors that are segregated into a corresponding plurality of sections which are electrically isolated from one another by a minimum distance based upon an

expected voltage difference between the sets of electrical conductors, each of the plurality of sets of electrical conductors being adapted for connection to a corresponding integrated circuit.

14. The package of claim 13, wherein the plurality of sections are segregated in accordance with a predetermined standard.

15. The package of claim 14, wherein the predetermined standard specifies a physical separation distance between conductors of the package based at least upon a voltage between the conductors.

16. The package of claim 13, wherein the first and second devices are semiconductor integrated circuit (IC) devices.

17. The package of claim 16, wherein the IC devices are communications devices.